UW-MFF E-Beam Silicon Photonics Layout Framework

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The UW MicroFabrication Facility provides a direct-write electron beam lithography process for fabrication of silicon photonics devices. This document describes design considerations for using this process, and the accompanying GDS-II data file is the preferred design framework for submitting pattern data for the 3-layer (full etch plus 2 partial-etch layers) silicon photonics e-beam build on a 25 mm SOI chip.

GDS-II Data Structure

Top Cell: **TOP**
Data Extent: (-12500, -12500) (12500,12500)

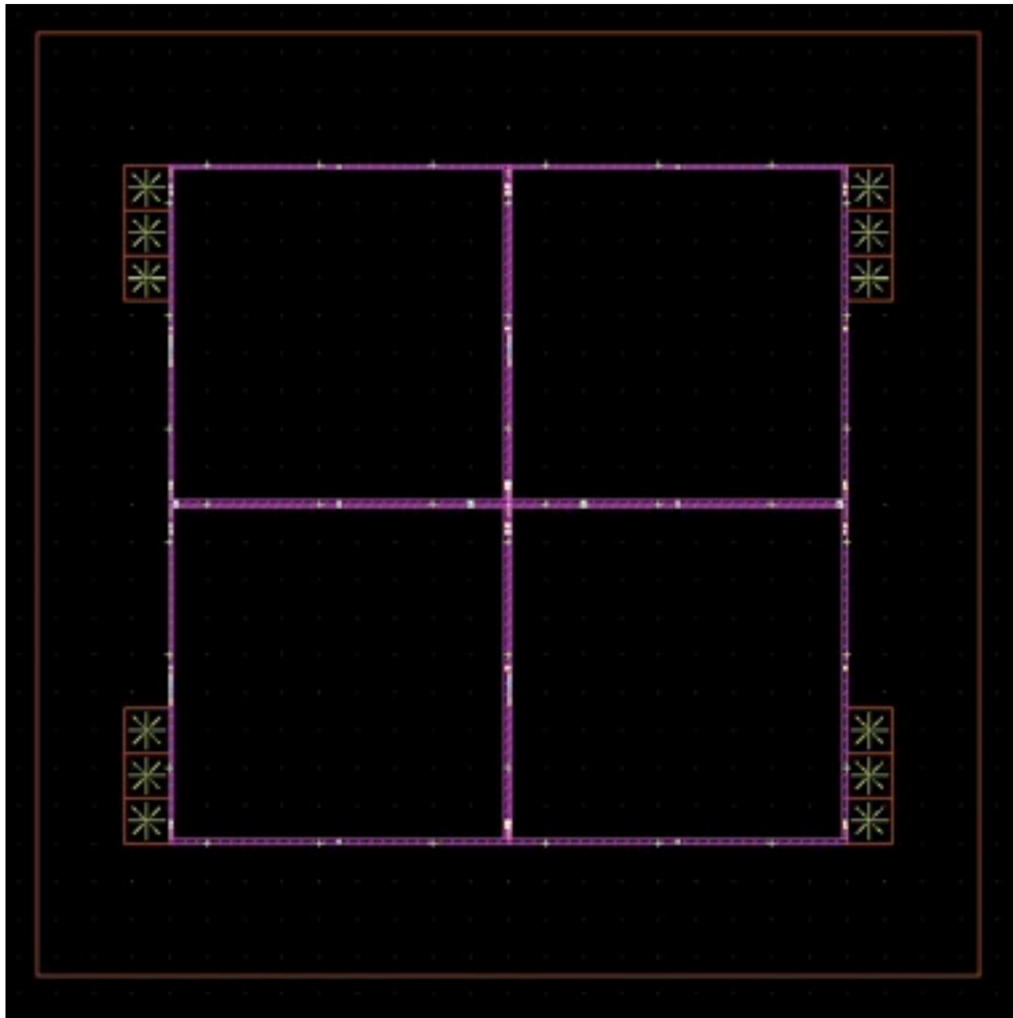
The framework provides maximum open area for device layout with required alignment and metrology features. Devices should be located in the four open regions; each is a structure in the data hierarchy: Data_LowerLeft, Data_LowerRight, Data_UpperLeft, and Data_UpperRight. In each of these 4 sub-cells, the cell/data origin is at the center, the open data area is 8800 x 8800 um, and the data extent is from (-4400,-4400) to (4400,4400). These data limits are represented by boxes on data layer 63. Keep your design within these boundaries. Alignment and process metrology structures are in the kerf regions, in structures prefixed “EB_”. Don’t modify anything in these cells, which are for e-beam alignment marks (MARKS), linewidth (CD), layer-to-layer overlay (OVL), and etch depth (ETCH).

Layer Assignments

You may place your data on any layers, but you must clearly communicate your layer assignments. You do not need to copy the data from these metrology layers into your own design layers.

GDS Layer	Contents
20	EBeam Zero (Marks) Layer
21	Ebeam Metrology for Layer 1 -- Full Etch Layer {Negative}
22	Ebeam Metrology for Layer 2 -- Partial Etch Layer 1 {Positive}
23	Ebeam Metrology for Layer 3 -- Partial Etch Layer 2 {Positive}
24	Dicing Marks (Optional)
25	Dicing Lanes (Layout Guides only, not exposed.)
63	Layout Borders (Layout Guides only, not exposed.)

Layout Image



Layer Polarity

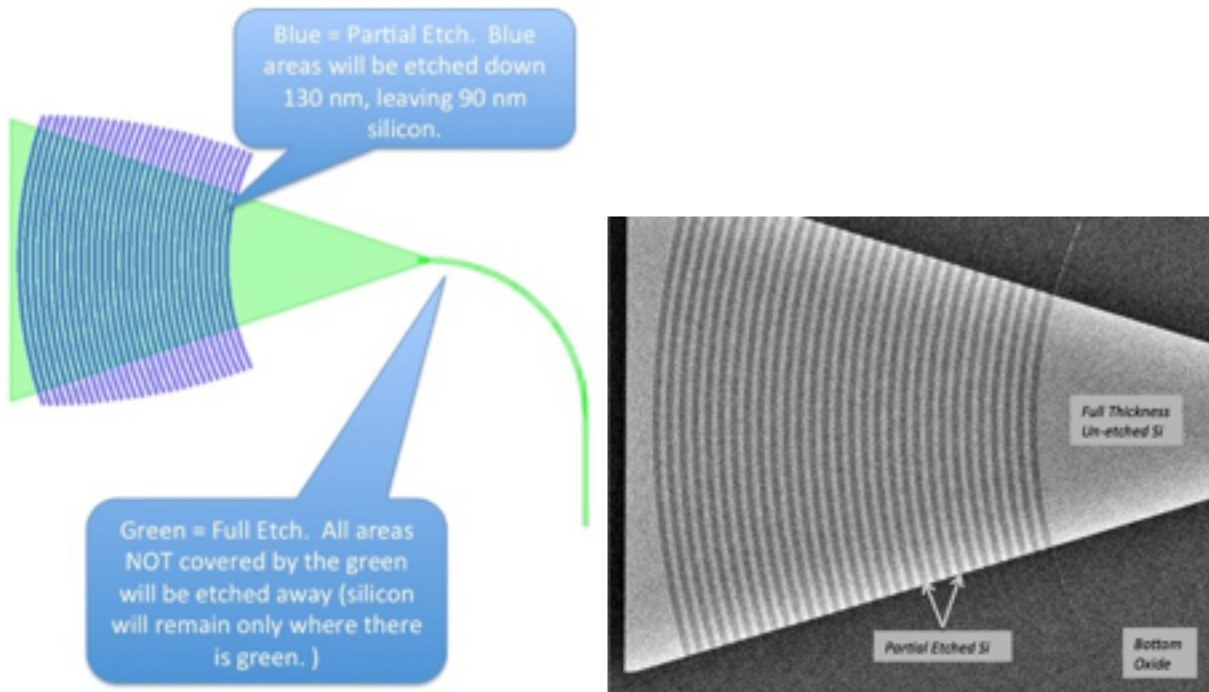
Fabrication will be most straightforward if you design for our process polarity. For typical designs, these polarities have smaller writing area, thus shorter writing time. We can do image reversals or bordering reversals, but these can occasionally be problematic, or can also result in impossibly large exposure areas.

Partial Etch Layer(s)

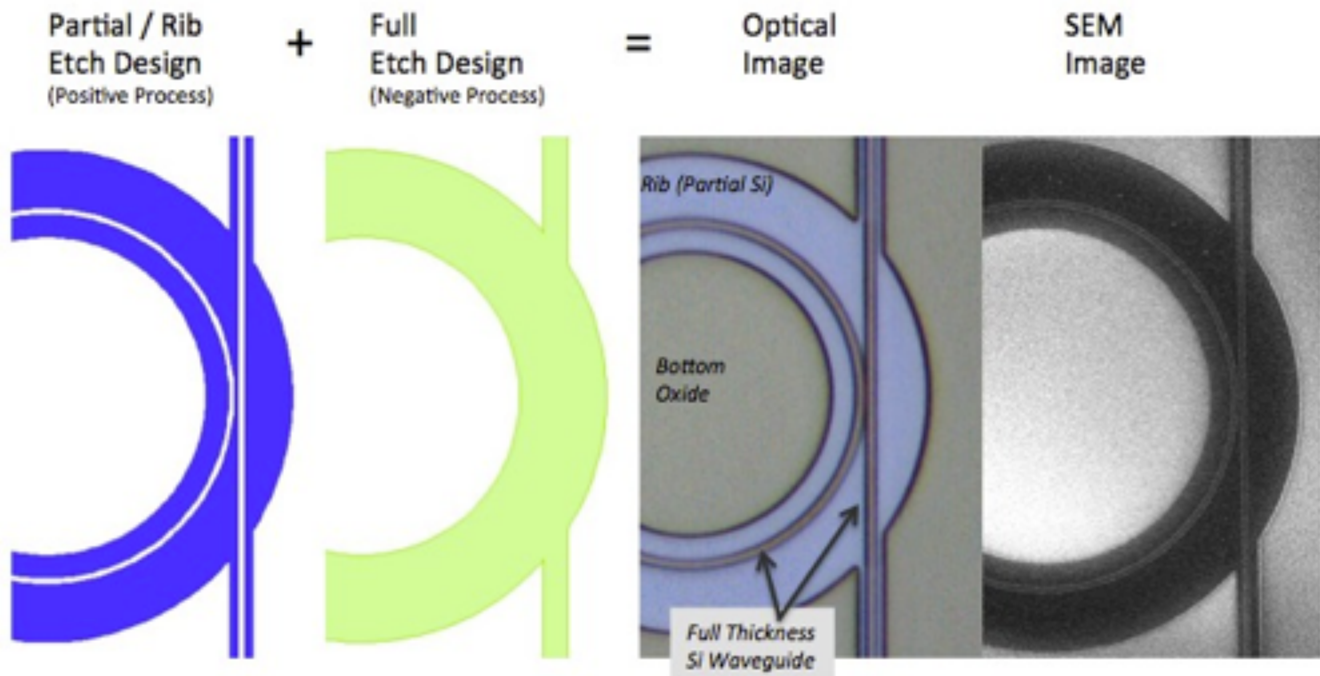
The preferred partial etch process is a positive resist process. For each partial etch layer, draw data in the areas you want to be partially etched. Draw solid shapes (rectangles, polygons) wherever you want the silicon to be the partial etch thickness, e.g. 90 nm thick / 130 nm deep etch. Areas outside the drawn data are not exposed, and will not be etched.

Full Etch Layer
For the full etch layer, draw data in the opposite polarity - draw data wherever you want the full silicon thickness to remain. Areas outside the drawn data are not exposed and will be etched away. Note that any areas you want to remain at the partial etch thickness must also be written by the full etch layer, or they will be etched away during the full etch.

Example 1. Partial-etched Grating Coupler
In this example, there is a full-height ridge waveguide and partial-etch grating coupler. After processing, the Full Etch layer shown in green will be full height silicon, the areas where there is both blue and green will be the Partial Etch thickness, and all areas not green will be etched away completely, including those areas which are blue but not covered by the green.



Example 2. Partial-etched Rib Waveguide
This example shows a full-height ridge waveguide with a partial-thickness rib etch on each side. After etching, any areas not exposed in the Full Etch (Green) layer will be etched away completely. Areas exposed in the Full Etch (Green) as well as the Partial Etch (Blue) layers will be etched to the partial etch depth, and areas exposed with the Full Etch (Green) but not the Partial Etch (Blue) will be un-etched and remain at the full silicon thickness.



Please discuss with us if these descriptions are not clear, or you would like to use a different polarity for your designs.

Design Considerations

Writing Time / Exposed Area
A primary concern when designing for e-beam lithography is written area. The time to write a pattern is directly related to the amount of exposed area, so to minimize write time, minimize the amount of written area.

Resolution / Minimum Feature Size / Writing Grid
Our e-beam process has quite a bit of flexibility for minimum feature size and placement grid (digitization), so we do not have a fixed specified minimum feature size or placement grid. There are complex trade-offs for resolution, writing grid, and writing time, so contact us to discuss your specific needs.

Layer Overlay
The layer-to-layer overlay error in our e-beam process typically averages about 30 nm across an SOI substrate, although results vary somewhat.