

Study of waveguide crosstalk in silicon photonics integrated circuits.

Valentina Donzella^{1*}, Sahba Talebi Fard¹ and Lukas Chrostowski¹

¹Department of Electrical and Computer Engineering, University of British Columbia, Canada

*corresponding author: valedonz@ece.ubc.ca

ABSTRACT

Silicon photonics is going through a terrific expansion driven by several applications, from chip wiring to integrated sensors and telecommunications. Some applications, e.g. intra and inter chip connections and sensing, require long parallel waveguides for wiring or for connecting grating couplers (GCs) to devices situated in sensing micro-channels. In well packed photonics chips there are often long wiring waveguides parallel for several mm, so loss can be caused by light coupled back and forth between them (cross-talk), by scattering, wall roughness, mode mismatch, etc. This work aims to investigate cross-talk for long parallel waveguides, and to propose methods to reduce cross-talk loss when high integration density is required.

We have designed and fabricated about 200 testing structures exploiting e-beam on silicon on insulator (SOI) chip, in order to test several parameters and to find out dominant loss mechanisms. All devices have been tested and measured using an automatic optical bench, in the wavelength range between 1500-1600 nm.

Achieved results are promising, since they allow for comparing cross-talk for short as well as long interaction lengths (up to 5 mm), different waveguide width pairs, several separation distances, and for TE and TM polarization. For smaller gaps, having not symmetric pair of waveguides is very beneficial, since it results in a lower power coupling, e.g. about 20/14 dB of crosstalk reduction for TE/TM waveguides after 5 mm of propagation and gap of 0.5 μm . This can be very useful for the design of integrated photonics chips requiring high-density packaging of devices and waveguides.

Keywords: Silicon Photonics, high-density photonics integration, Silicon on Insulator SOI, integrated optics, waveguide cross-talk, directional couplers, optical bio-sensors.

1. INTRODUCTION

Industry and governments have recently invested and promoted Silicon Photonics, contributing remarkably to its sudden and quick development¹. In addition to these investments, commercial state-of-the-art CMOS foundries have started proposing and testing monolithic optoelectronic (OE) integration. The preliminary results of all these efforts have pointed out that silicon photonics has the potential to be truly CMOS compatible. Many different groups have developed and demonstrated several components in CMOS compatible technology, such as integrated Silicon electro-optic modulators², ultrafast Ge-on-Si photodetectors³, efficient fiber-to-waveguide couplers⁴, and Si Raman lasers⁵. Further active and tunable silicon photonics devices and sensors are under investigation, exploiting several different approaches, and commercial fabrication processes are becoming mature and reliable⁶. The new paradigm for the Si-based photonics and opto-electrics is that their complex circuits will be entirely integrated onto chips. Those circuits, properly designed and optimized, will operate on a broad spectral wavelength range, from 1.2 μm up to 100 μm , with cryo-cooling needed in some cases.

This quick development and expansion of silicon photonics devices and applications has seen silicon photonics chips becoming more and more filled with devices, with high-density of integration and thousands of devices and waveguides packed close together, pushing technological rules and physical limits. In some cases, parallel long waveguides are required for routing or connecting devices, causing additional losses (further to waveguide loss, more details will be provided in the next paragraph) due to parasitic coupling, or cross-talk, between them. Obviously, the closer the waveguides, the more is their interaction, but on the other hand, the farther parallel waveguides are placed, the more is the area wasted only for routing. For example, chips for bio-applications require grating couplers (GCs) for coupling light in/out to/from the chip to be at least 5 mm apart from the actual sensing devices, to allow for bonding PDMS with microfluidic channels on top of the sensors without covering GCs, Fig. 1^{7,8}. Assume to have 100 sensors in channel, and each device is connected by two regular waveguides (500 nm width) only to two GCs, one for interrogation and one for

response reading. In this case the area needed for routing is at least 3.5 mm^2 , if routing space is $3 \mu\text{m}$, but it can be reduced to only 1.5 mm^2 if spacing between waveguides is reduced to $1 \mu\text{m}$. In table 1, the area allocation for routing is evaluated, considering a chip with a surface of 50 mm^2 , and hypothesizing to have 100 or 1000 devices on it. It is clearly shown that increasing the number of devices the space allocated for routing increases remarkably, so having a clear picture of cross-talk between waveguides and system noise requirements is fundamental to have a proper area allocation on chip.

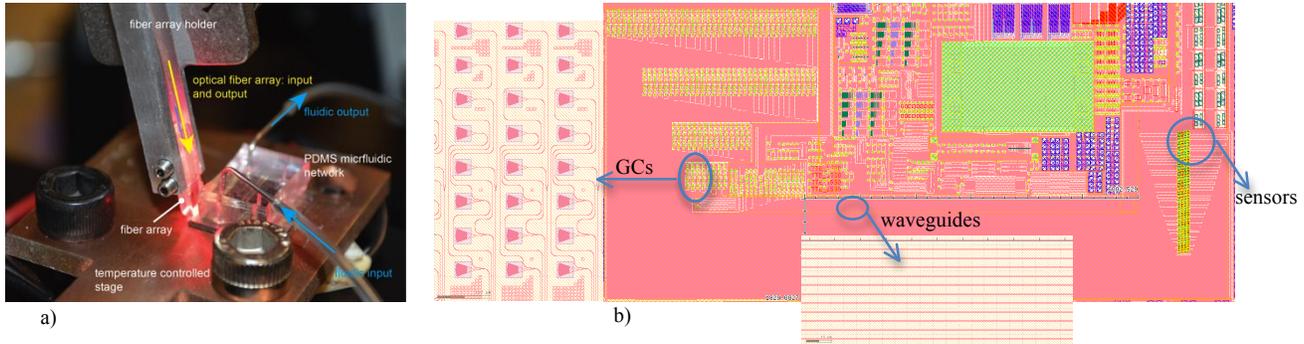


Figure 1. a) Picture of measurement setup. Since the PDMS block is bonded on the chip the fiber array can get only GCs, which are few mm away from devices in fluidic channel. This requires a proper design, which is shown in b). GCs related to fluidic devices are on the left side of the chip, while sensors are on the right side, and they are connected by several 5-6 mm long parallel waveguides.

Table 1. Area used for waveguide connection (5 mm long) on chip (e.g. of 50 mm^2 surface) depending on waveguide spacing

Number of devices	100		1000	
	3 μm	1 μm	3 μm	1 μm
Waveguide spacing	3 μm	1 μm	3 μm	1 μm
Area for routing	3.5 mm^2	1.5 mm^2	35 mm^2	15 mm^2
% of chip area	3	7	30	70

This paper aims to give insight about waveguide cross-talk in highly integrated silicon photonics circuits, analyzing causes of loss and proposing possible solutions or/and system improvements. In the next paragraph the fundamental causes of waveguide loss will be reviewed, with a more detailed analysis of parasitic coupling between parallel waveguides. Then material and methods used for designing the test structures and for their measurements will be described and finally some preliminary results and comparison between experiments and analysis will be discussed, in order to give some indications for the design of highly-packed Silicon Photonics chips.

2. WAVEGUIDE LOSS

Light propagation in waveguides is unavoidably associated with several kinds of loss. Some of them are associated to the media itself that is guiding the propagation, while some others are associated to the technological process and some imperfections and can be reduced by improving the process itself. Equation 1⁹ summarizes the main causes of loss in Silicon on Insulator (SOI) waveguides.

$$L_{\text{tot}} = L_a + L_{\text{ss}} + L_{\text{vs}} + L_{\text{cs}} \quad (1)$$

In the above equation, L_{tot} is the total waveguide loss for a straight waveguide, and is usually expressed in dB/cm (so the longer the waveguide the higher the loss). The term L_a is the material absorption loss, for undoped silicon, at $\lambda=1523 \text{ nm}$, $L_a=0.004 \text{ dB/cm}$ ¹⁰. This kind of loss cannot be avoided, but it is clearly a small contribution (e.g. for a 5 mm long waveguide it results in 0.02 dB loss), it is wavelength dependent and increases in the case of silicon doping. L_{ss} is the interface induced scattering, it depends on the fact that the field is mainly propagating in the material with higher

refractive index but its evanescent field extends also in the cladding. Scattering amount is proportional to $E_s^2(n_2^2 - n_1^2)$, namely the intensity of electromagnetic field on waveguide surface, and the difference between squared refractive indexes of waveguide core and cladding. Scattering also depends proportionally on another factor, which can be called R^2 , where R is the r.m.s. roughness of waveguide surface¹¹, and this is clearly associated to sidewall etches as well as interfaces between Si and SiO₂¹². Scattering is usually more associated to sidewall loss than to top/bottom interfaces, since the etch step is a main source of roughness, and for this reason this kind of loss affects the first TE mode more than first TM¹². Another source of loss during propagation is L_{vs} , which is related to volumetric variations of the refractive index. Those are intrinsic in the process of wafer manufacturing, since implanting and growth have the potential of creating islands of impurities and crystals defects. Finally, L_{cs} is the loss due to the coupling of propagating modes with substrate modes. In a typical SOI chips, the lower SiO₂ waveguide cladding is chosen 2 μm thick to reduce this kind of mode coupling in the third telecommunication window.

As just explained, L_{tot} is the total loss associated to light propagating in a straight waveguide, but there are additional sources of loss. One of the most relevant is bending the waveguides, that obviously is needed to have suitable waveguide connections, and the other one is mode coupling due to light travelling in parallel waveguides.

Concerning bend loss, the main source of extra loss is mode-mismatch between mode in straight waveguide and mode in the bend. This mismatch causes reflection (at the interfaces between straight and bent waveguides) and thus power dissipation, and the effect is more dramatic for smaller curvature bends. Plus, some extra loss may be induced by an increased interaction between the mode and outer sidewall, since light is pushed towards it in the bend^{14, 15}.

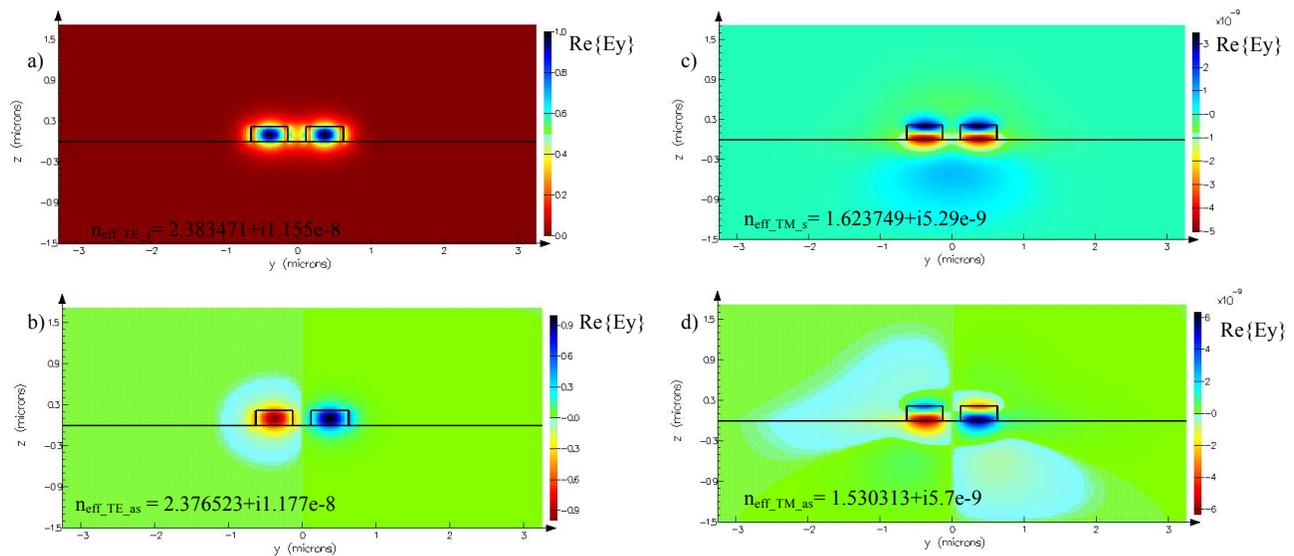


Figure 2. Transverse cross-section of two parallel waveguides (gap side by side is 250 nm) and effective indexes of plotted modes. Waveguide is silicon made, width=500nm, height= 220nm; top cladding is air while bottom cladding is a 2 μm thick silicon dioxide layer on the top of silicon substrate. a) and b) are symmetric and a-symmetric mode for the first TE mode, while c) and d) are symmetric and a-symmetric mode for the first TM mode.

Finally, as we have stated in the introduction, high-density integration of devices on photonics chips as well as specific design requirements (as in bio-applications) may cause to have packed parallel routing waveguides, inducing extra loss due to mode coupling between them. If the parallel waveguides are identical (i.e. same materials and geometries), power exchange between them is periodic and complete, and its period depends on geometry, materials and light polarization. This interaction between the waveguides causes the formation of the so-called structure super-modes and it is possible only if the two waveguides are close enough, where close enough again depends on geometrical and physical properties of waveguides/light. With super-modes we indicate the modes of the total system, made up by the two interacting waveguides. In general each mode of the single waveguide is split into two super-modes of the total system, and these two super-modes, one symmetric and one anti-symmetric (Fig. 2), have slightly different effective indexes, $n_{\text{eff-s}}$ and $n_{\text{eff-as}}$. A proper combination of total system super-modes can describe the total light field propagating in the system itself, as summarized in equation 2. On the other hand, when the parallel waveguides are far enough, they can be considered as independent one from the other and can be described as separate waveguides (and if identical, they will

have the same effective index for each propagating mode, slightly different from the one of symmetric and anti-symmetric modes).

$$\Psi(x) = c^+ e^{-j\beta^+ x} \left(\phi^+ + \phi^- e^{j(\beta^+ - \beta^-)x} \right) \quad c^+ = c^- = 1/\sqrt{2} \quad (2)$$

In equation 2, $\Psi(x)$ is the total field propagating into the system along x direction, while ϕ^+ and ϕ^- are the symmetric and anti-symmetric modes respectively, with their propagation constants, β^+ and β^- . The two coefficients c^+ and c^- are the weights for the two super-modes, which are equal in the case of identical waveguides. If we consider to have light injected only in one of the waveguides, with an input power P^0 , we can define the power transmission and coupling coefficients, respectively t^2 and k^2 , as shown in equation 3. The power exchange between the two waveguides is periodic and linked to their geometry by the coefficient c , which is proportional to the difference in the effective indexes of the two super-modes under analysis ($\Delta n = n_{\text{eff}_m1_s} - n_{\text{eff}_m1_{as}}$).

$$k^2 = P^-/P^0 = \sin^2(cx); \quad t^2 = P^+/P^0 = \cos^2(cx) \quad c = \pi\Delta n/\lambda \quad (3)$$

Input light is fully coupled to the second waveguide when the coupling coefficient is maximized, the distance travelled by the light is called cross-over length, L_c , and it can be evaluated using equation 4. Power coupled can be written as a function of L_c itself, as shown in equation 5. Thus, if the coupler length, x , is orders of magnitude smaller than L_c , the power coupled is very low, of the order of less than -50dB.

$$L_c = \lambda/(2*\Delta n) \quad (4)$$

$$k^2 = \sin^2(\pi*x/(2*L_c)) \quad (5)$$

In figure 3 a plot of cross-over length for the first TE and TM mode is shown, in typical Silicon strip waveguides (500nm wide and 220 nm high), and for different waveguide separations. The gap is intended side by side. The cross-over length increases when the separation between the waveguides becomes wider, this in turn means that the power coupled can be reduced significantly when L_c becomes significantly greater with respect to the coupler length (that on a chip can be of the order of few mm for an optical connection).

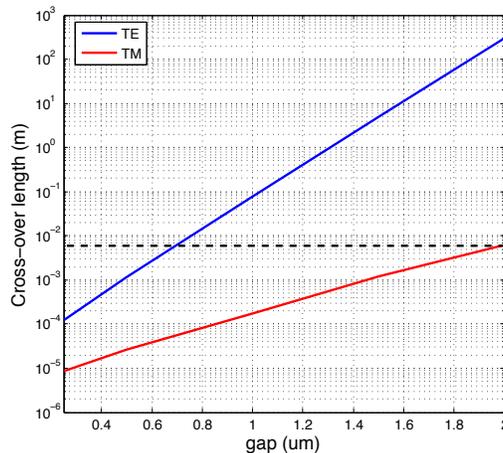


Figure 3: Cross-over length (defined in Eq. 4) for the first TE (blue plot) and TM (red plot) modes in a standard Silicon photonics waveguide (500nm wide x 220nm high) versus the gap (side by side) between two parallel waveguides of the same type. The dotted line indicates 5 mm length, which is a typical connection length on a bio-chip.

In the case of not identical waveguides, we can still talk about system super-modes, but there is no formation of properly symmetric and anti-symmetric modes. For this reason there is not complete power coupling to the second waveguide, but only a small fraction of the input power is coupled to the second one. In this case light propagating in the system can be described by equation 6, but unlike Eq. 2, the coefficient c^+ is not equal to c^- .

$$\Psi(x) = c^+ e^{-j\beta^+ x} \left(\phi^+ + \frac{c^-}{c^+} \phi^- e^{j(\beta^+ - \beta^-)x} \right) \quad (6)$$

3. METHODS AND MATERIALS

The coupling between parallel waveguides has been simulated using an eigenmode solver (Lumerical MODE Solutions) and the finite difference time domain method (Lumerical FDTD Solutions) in order to find out system super-modes and effective indexes and to observe properly the coupling between the waveguides. FDTD simulations allow us to monitor the power that is travelling into the two waveguides, so it is a very powerful mean to check design parameters and to understand how power exchange takes place. In Figure 4a and b, we plotted the first and the second mode on the transverse cross-section of the system made up by two not identical waveguides (width of the first one, w_1 , is 500 nm, and width of the second, w_2 , is 450 nm), and in Fig. 4c, we plotted the power propagating in each one of them, after light has been injected in the first waveguide. Mode profiles are calculated using MODE, while the propagation analysis has been done using FDTD. It is clear that the case reported in Fig. 4 is different from the ones reported in Fig. 2, since now the modes are more similar to the fundamental modes of the two independent waveguides. Those two different modes are also partially present in the adjacent waveguides, but this is due only to an overlap of the evanescent field with the second waveguide cross-section. From power propagation, we can estimate the coupling length (which is very low compared to the same case for identical waveguides, i.e. about 60 μm versus about 110 μm , for the first TE mode and gap of 250 nm) as well as estimate the coupling strength, that is much smaller compared with the full coupling in the case of identical waveguides. The values from simulations were used to design proper test structures for cross-talk between long parallel waveguides.

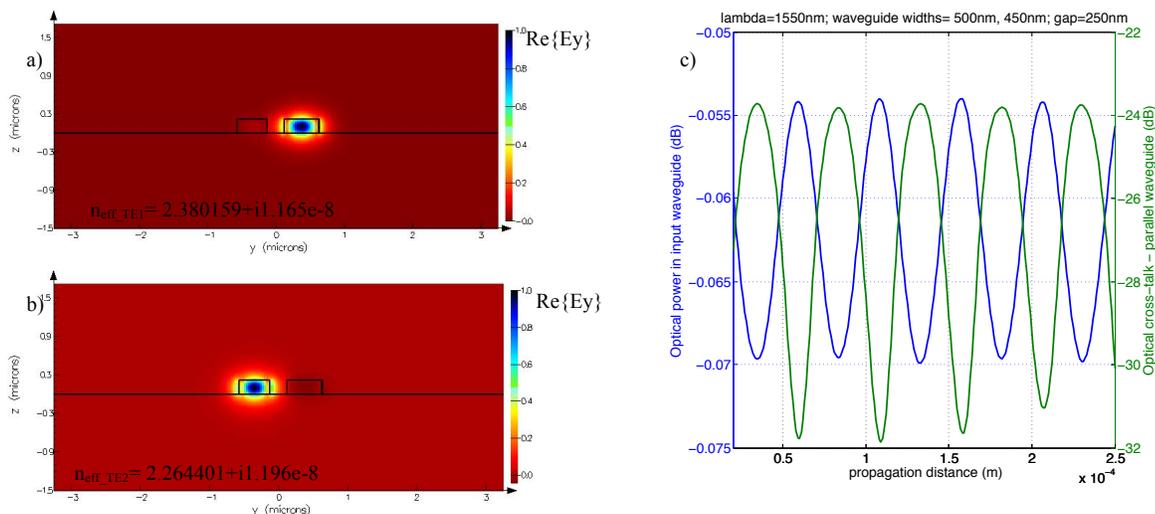


Figure 4. Transverse cross-section of two parallel waveguides (gap side by side is 250 nm, $w_1=500\text{nm}$, $w_2=450\text{nm}$) and effective indexes of plotted modes. Waveguide is silicon made, height is 220nm; top cladding is air while bottom cladding is a 2 μm thick silicon dioxide layer on the top of silicon substrate. a) and b) are the first two TE modes of the system. c) The plot represents the power travelling in the input waveguide (blue curve) and the power coupled to the second waveguide (green curve). In this case the maximum power coupled is very low, about -24 dB.

The test structures have been fabricated on Silicon on Insulator (SOI) chip, in the University of Washington's Microfabrication Facility (MFF) using a JEOL JBX-6300FS Direct Write E-Beam Lithography System (EBL) (Peabody, MA). The EBL provides a low-cost, fast turn-around, foundry-compatible fabrication alternative that has been optimized¹⁶⁻¹⁸ to produce consistent, robust, low-loss silicon photonic components¹⁹, making the transition to a costly foundry service with high confidence. Several test structures have been fabricated, for TE and TM polarization and for the case of identical pair of waveguides and not identical pair. Structures for five different gaps have been designed and fabricated, with different length of the coupler, having a maximum coupling length of 5 mm.

The optical test setup is partially shown in Figure 1a. Equipments are controlled via PC, to orchestrate stage position, alignment, laser, detectors and, in the case of biological experiments, reagents sequencing. The optical devices are characterized using a tunable laser source (Agilent 81682A, with an output wavelength range from 1460 to 1580 nm) and optical power sensors (Agilent 81635A); temperature controller (SRS LDC501); microscope; and computer for data acquisition. Light is coupled on and off chip using a four-port polarization maintaining optical fiber array (PLC

Connections, Columbus, OH). The fibers interface to on-chip grating couplers²⁰ designed to couple light into either TE or TM waveguide modes. GCs are then properly connected to test structures.

4. RESULTS

The fabricated test structure layout for cross-talk measurements is shown in Fig. 5. Each test structure has 2 inputs and 2 outputs, so during measurements it has been possible to monitor simultaneously the two output powers injecting light only in one waveguide. In this way we can monitor the light that is parasitically coupled to the second waveguide as well as the light that is actually propagating in its own waveguide. Adiabatic bends have been used in the layout in order to reduce power coupling from bend radiation loss. Fig. 5 c) shows the rough output data for a TE test structure, identical waveguides and a separation gap of 500 nm, total coupling length is 5 mm. Once, the alignment of fiber array has been adjusted and tested, all the test structures have been measured exploiting the automated setup described in the previous paragraph. The rough data are properly filtered and analyzed using Matlab.

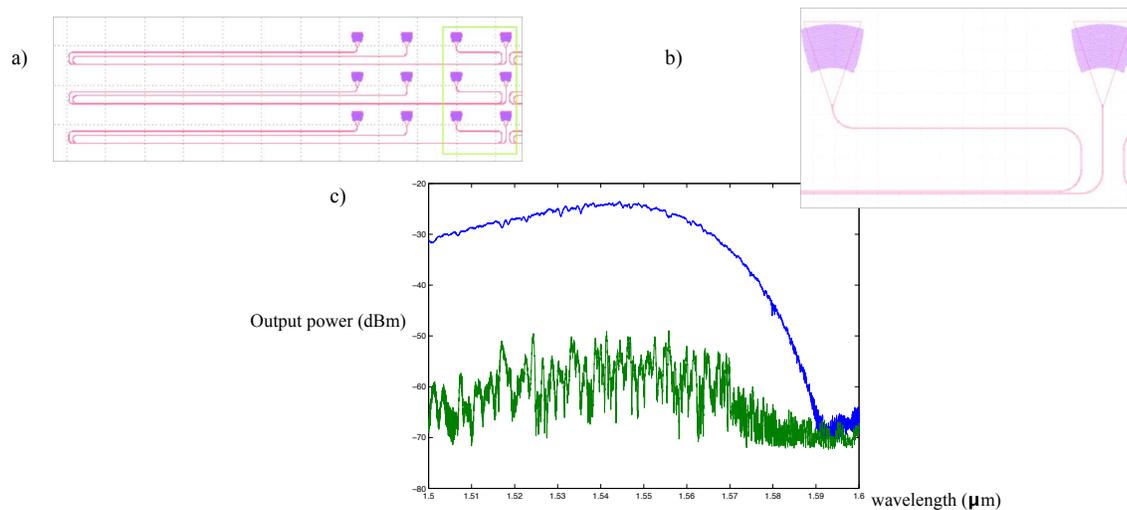


Figure 5: a) (1 division is 100 μm) and b) layout masks for the fabrication of the test structures, pink shapes represent the residual Silicon waveguides. a) shows the entire structure with its two inputs and two outputs while b) is a detail with the GCs and the coupling region. c) rough output plot with power in the two channels versus wavelength (blue curve is the output channel where light has been injected, while green is cross-talk in second waveguide), the curvy shape is due to the frequency response of the GCs, whose response is maximized at 1550 nm.

Showing all collected data is outside the scope of this paper, but we would like to focus the attention on the cross-talk loss resulted for the longer test structures (5 mm length). The comparison between measured and simulated data is reported in Fig. 6, for both TE and TM polarization.

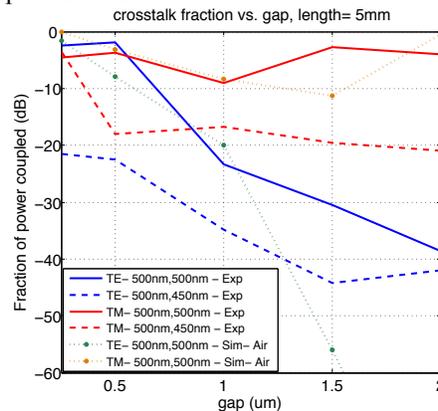


Figure 6: Coupling cross-over between 5 mm long parallel waveguides for TE and TM mode. The plot compares measured results (with label “Exp” in legend) for identical waveguide pairing versus not-identical pairing as well as simulated results (with label “Sim” in legend).

The plot shows that having not-identical pairs is beneficial, since it remarkably reduces the cross-talk, in particular for smaller gaps. For example, with a small waveguide spacing, i.e. 500 nm gap side by side, the coupling of TE mode is reduced of about 20 dB in measurements and of about 14 dB for TM mode. In addition, TE mode has a cross-over length (for gaps that are larger than 1 μm , see Fig.3) that is orders of magnitude longer than the test structure length, thus the amount of power coupled decreased dramatically for larger gaps. Theoretically, the expected cross talk decrease is more than the measured one, but it is worth noticing that in these cases measurements are limited by receiver noise-floor. On the other hand, for TM mode the cross-over length is smaller than test structure length, and only for 2 μm gap is comparable with it, so more coupling is expected and measured. If the gap is increased, the expected power coupling from simulations drops as well, e.g. for a gap of 3 μm expected power coupling is less than -40 dB. It is clearly shown in Fig. 6, that even for TM mode, having not-identical waveguide pairing reduces sensibly the power coupled (this is true for gap larger than 250 nm).

From the above considerations and depending on the loss affordable by the design, each one can choose waveguide spacing depending on several factors, and first of all the polarization. It is evident that if less than 40 dB of parasitic coupling between parallel waveguides is the target of the chip design, TM waveguides will require a gap larger than 2 μm . If several waveguides are required to be parallel for long segments, using not-identical waveguide pairing is highly beneficial, for both TE and TM mode, it allows to use smaller spacing and it could be straight forward to be done in the design phase, using for example automatic routing tools. One final remark goes to fabrication reliability, indeed, if the process has high radiation loss from waveguides, this can for sure have a detrimental effect, increasing cross-talk, in particular for smaller gaps.

5. ACKNOWLEDGEMENTS

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REFERENCES

- [1] Soref, R. "The past, present, and future of silicon photonics." *Selected Topics in Quantum Electronics, IEEE Journal of* 12.6 (2006): 1678-1687.
- [2] Xu Q., Schmidt B., Pradhan S., Lipson M., "Micrometre-scale silicon electro-optic modulator", *Nature* 435 (2005): 325-327
- [3] Michel J., Liu J., Kimerling L.C., "High-performance Ge-on-Si photodetectors", *Nature Photonics* 4.8 (2010): 527-534.
- [4] Dong, P., et al. "High-speed and compact silicon modulator based on a racetrack resonator with a 1 V drive voltage." *Optics letters* 35.19 (2010): 3246-3248.
- [5] Liang D., Bowers J.E., "Recent progress in lasers on silicon." *Nature Photonics* 4.8 (2010): 511-517.
- [6] Ding, R., et al. "A silicon platform for high-speed photonics systems." *Optical Fiber Communication Conference. Optical Society of America*, 2012.
- [7] Fard, Sahba Talebi, et al. "Label-free silicon photonic biosensors for use in clinical diagnostics." *SPIE OPTO. International Society for Optics and Photonics*, 2013.
- [8] Grist, Samantha M., et al. "Silicon photonic micro-disk resonators for label-free biosensing." *Optics express* 21.7 (2013): 7994-8006.
- [9] Rickman, A. G., G. T. Reed, and Fereydoon N. "Silicon-on-insulator optical rib waveguide loss and mode characteristics." *Lightwave Technology, Journal of* 12.10 (1994): 1771-1776.
- [10] Swimm, R. T. , "Optical absorption in the band gap in high purity silicon," in *Basic Properties of Optical Materials, Presented at the Topical Conference on Basic Properties of Optical Materials, Vol. OM85, Albert Feldman, Ed. Washington, DC: U.S. Dept. Commerce/National Bureau Standards Spec. Pub. #697, pp. 158-159, 1985.*
- [11] D. Marcuse, *Light Transmission Optics*. 2nd ed., Van Nostrand Reinhold, 1982, pp. 380 and 396.
- [12] Tymon, B., and Smith, H.I. "Evolution of line-edge roughness during fabrication of high-index-contrast microphotonic devices." *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* 21.6 (2003): 2892-2896.

- [13] Vlasov, Y.A., and McNab, S.J., "Losses in single-mode silicon-on-insulator strip waveguides and bends." *Opt. Express* 12.8 (2004): 1622-1631.
- [14] Marcatili, E. A., "Bends in optical dielectric guides," *Bell Syst. Tech. J.* 48, 2103 (1969).
- [15] Chrostoski, L., and Hochberg, M., "Silicon Photonics Design", book (2013).
- [16] Sardo, S., et al., "Line edge roughness (LER) reduction strategy for SOI waveguides fabrication," *Microelectronic Engineering* 85, 1210-1213 (2008).
- [17] Gnan, M., et al. "Enhanced stitching for the fabrication of photonic structures by electron beam lithography." *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures* 25.6 (2007): 2034-2037.
- [18] Chen, Y., et al. "Simple technique to fabricate microscale and nanoscale silicon waveguide devices." *Frontiers of Optoelectronics in China* 2.3 (2009): 308-311.
- [19] Chen, Y., et al. "Fabrication of silicon microring resonator with smooth sidewalls." *Journal of Micro/Nanolithography, MEMS, and MOEMS* 8.4 (2009): 043060-043060.
- [20] Mekis, Attila, et al. "A grating-coupler-enabled CMOS photonics platform." *Selected Topics in Quantum Electronics, IEEE Journal of* 17.3 (2011): 597-608.