Electron beam lithography writing strategies for low loss, high confinement silicon optical waveguides

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The authors present a robust process for fabricating passive silicon photonic components by direct-write electron beam lithography (EBL). Using waveguide transmission loss as a metric, we study the impact of EBL writing parameters on waveguide performance and writing time. As expected, write strategies that reduce sidewall roughness improve waveguide loss and yield. In particular, averaging techniques such as overlap or field shift writing reduce loss, however, the biggest improvement comes from writing using the smaller field-size option of our EBL system. The authors quantify the improvement for each variation and option, along with the tradeoff in writing time. © *2011 American Vacuum Society*.
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I. INTRODUCTION

Silicon photonics has diverse applications including, among others, nano-optomechanics,[1] biosensing,[2] nonlinear optics,[3] and long-wavelength integrated photonics.[4] There are now foundries offering silicon photonics fabrication of increasing complexity, with the aim of fully integrating CMOS logic and photonic devices.[5–7] To complement the foundry services a desirable capability is reliable rapid prototyping; for example, to verify device models or study a wide range of design variations. For this reason, we have established a robust process for the fabrication of simple silicon photonic components, using direct-write electron beam lithography (EBL) and inductively coupled plasma (ICP) etching of silicon. Here we report our baseline performance, and our exploration of a range of design and fabrication parameters of the EBL process.

A key distinction from most prior waveguide loss studies is the use of an automatic wafer-scale optical probing system, which allows for the unattended measurement of hundreds or even thousands of waveguides. With a large volume of data, we can distinguish even small performance changes with statistical confidence. It would not be feasible to measure such a large number of devices using edge coupling, which would require cleaving and/or polishing, and individual manual alignment of each device.

Fundamental to our goal of advancing the state-of-the-art in silicon photonics devices, we must produce consistent fabrication results over time, which, in turn, requires the development of a simple, robust, and reliable fabrication process, which is often challenging in a university environment. These aims are met not only by maximizing the latitude of each process step but also by minimizing process content. Adding process steps may improve some performance metrics, but will likely increase process variability and decrease reliability in a university setting with poor process control.

The primary determinant of loss in planar silicon waveguides has been shown to be sidewall roughness.[8,9] Therefore, our process development has been geared toward minimizing both resist and etch edge roughness. We found it difficult to reliably quantify physical sidewall roughness with our equipment set, and have subsequently relied solely on waveguide loss measurements to guide process optimization.

II. EXPERIMENT

A. Baseline process

Our baseline single-layer silicon photonics process begins with silicon-on-insulator (SOI) material, either 205 or 220 nm thick silicon, on 3000 nm thick silicon dioxide. Substrates in this study were 25 mm squares cleaved from 150 mm wafers. After a solvent rinse and hotplate dehydration bake, hydrogen silsesquioxane resist (HSQ, Dow-Corning XP-1541-006) is spin-coated at 4000 rpm, then hotplate baked at 80 °C for 4 min. Electron beam lithography is performed using a JEOL JBX-6300FS system, operating at 100 kV energy, 2 nA beam current, and 500 μm exposure field size. The machine grid, used for shape placement, is 1 nm, while the beam stepping grid, which is the spacing between dwell points during the shape writing, is 4 nm. An exposure dose of 2800 μC/cm^2 is used, which we found to give both optimal waveguide performance along with dose-to-size for most features. After exposure, the resist is developed by immersion in 25% tetramethylammonium hydroxide for 4 min,[10] followed by a flowing deionized water rinse for 60 s, an isopropanol rinse for 10 s, and then blown dry with nitrogen. The silicon is then removed from unexposed areas using inductively coupled plasma etching in an Oxford Plasmalab System 100, using a chlorine gas flow of 20 sccm, pressure of 20 mT, ICP power of 800 W, bias power of 40 W, and platen temperature of 20 C, resulting in a bias voltage of 185

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V. During etching, chips were mounted on a 100 mm silicon carrier wafer using perfluoropolyether vacuum oil.

This process has been shown to be consistent over time and highly robust to the variation of key process parameters. It produces reasonably smooth sidewalls with a slope of 82°. Typical SEM micrographs are shown in Fig. 1. Although sidewall roughness and thus, waveguide loss could be further reduced with the addition of process steps such as oxidation,[11,12] hydrogen annealing,[13] or laser reformation,[14] we have avoided adding any additional steps that might increase process variability.

For measurement, the waveguides are clad by spin-coating 950K average molecular weight poly(methyl methacrylate) (PMMA) to a thickness of 2 μm. Measurements are performed on a custom-built wafer probing system consisting of a wafer translation stage, an optical fiber array positioned above the wafer surface for coupling of light into and out of the wafer plane, a tunable laser, and a detector.[15] Computer control positions the wafer stage at each device to test, performs fine alignment of the fiber array to the grating couplers with optical feedback, then sweeps the wavelength of the laser source, recording power output.
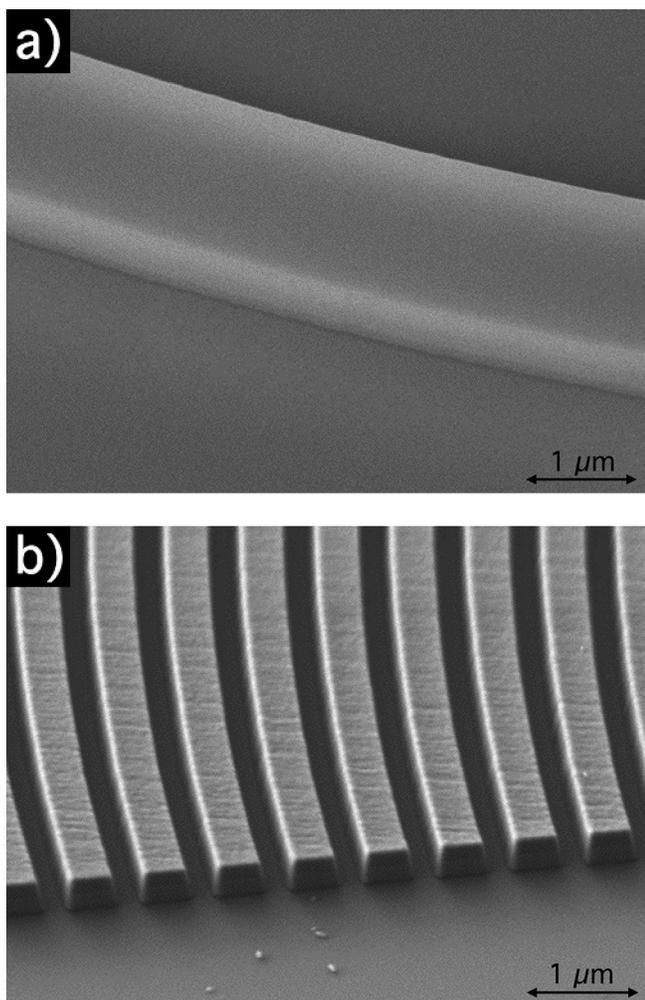
To evaluate process performance, we designed a simple test cell, shown in Fig. 2. This cell size is 1.1×2.7 mm^2, and contains three types of elements: (1) grating coupler test structures, for measurement of the insertion loss to grating couplers, (2) 400 nm wide straight ridge waveguides in 5 lengths from 1.5 to 9.7 mm, and (3) 400 nm wide curved ridge waveguides, also in 5 lengths. The transmission of each individual waveguide is measured and the loss per unit length is determined from a linear fit of loss against length.

In this study, each chip contained between 50 and 120 instances of the test cell, with 3 to 6 parameter variations, but always with at least 8 die at each test condition. We report data from a total of 484 die, or 4840 individual waveguides.

B. Parameter variations

With an established baseline process, we next explored the impact of various parameters on the waveguide results. For each variable explored, all variations were exposed on the same substrate, with positions distributed to avoid any possible positional effects.

The first parameter evaluated is in the generation of the pattern design file itself. The industry-standard GDS-II

FIG. 1. Scanning electron microscope images demonstrating our baseline process, for the (a) ridge waveguide, and (b) grating coupler.
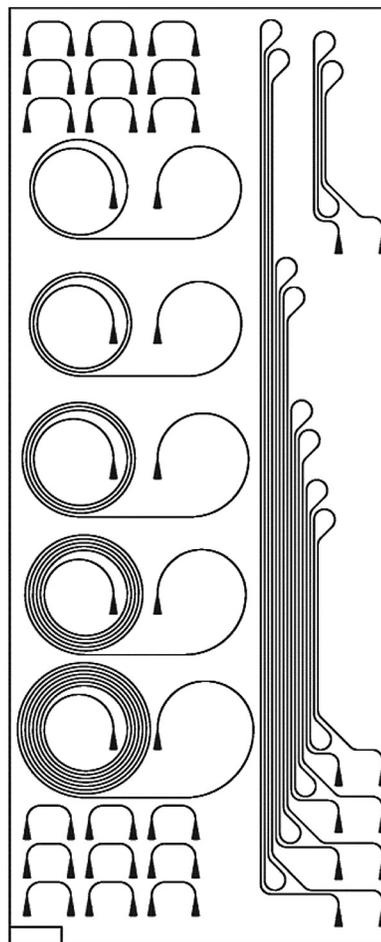

FIG. 2. CAD layout for the waveguide test cell, containing grating coupler test arrays, and 5 lengths each of linear and curved waveguides.

design format does not support curved primitives, so curved shapes must always be piecewise approximated by polygons, which are subsequently fractured into primitive rectangles and trapezoids for e-beam writing. To evaluate digitization effects, we designed waveguides using 600 and 2400 points-per-circle, as shown in Fig. 3, corresponding to angular increments of 0.6° and 0.15°, respectively. For a curved waveguide of radius 160 μm, the deviation from the ideal curve in the 600-point polygon approximation is as much as 3.5 nm, whereas in the 2400-point approximation, the maximum error is less than 0.3 nm.

We then evaluated the fundamental EBL writing parameters of exposure grid spacing, beam current, and field size. Grid spacing, or shot pitch, is the distance between beam dwell locations during shape writing. We exposed a range of shot pitches from 2 to 32 nm. We then evaluated the waveguides written using beam current values of 2 and 8 nA. The JBX-6300FS has two exposure field sizes available, corresponding to the system's two objective lenses. Our baseline process uses the standard, or high-speed lens, referred to as "4th lens," which has a field size of 500 μm and a 1 nm machine or shape placement grid. We also evaluated the nanolithography or "5th lens" mode, which has a shorter working distance, smaller field size of 62.5 μm, and a 0.125 nm machine grid.

We evaluated several averaging techniques available in the JBX-6300 system. The first is overlap writing, in which pattern areas are written not just once, but are re-written multiple times in succession, with a resulting reduction in noise by temporal averaging of the system and environmental noise components. To maintain the exposure dose, when each shape is re-written n times, the pixel dwell time for each pass is reduced by 1/n of the total dwell time. A more advanced averaging mode, called field-shift writing, furthers

the concept by averaging not only multiple overlapping re-writes, but also by moving the exposure stage by one-half of the field size in both x and y axes between writing passes of the shapes. This averages not only temporal noise components but also spatial aberrations of the deflection system, including field stitch boundaries, since each shape is now partially written by different areas of the exposure field.

To quantify the effect of field stitching errors on waveguide loss, intentional offsets of varying dimension were programmed into the design of the waveguides to measure the additional loss due to these stitching errors. Programmed stitching errors ranged in magnitude from 0 to 32 nm. In this experiment, only the shear or offset component of the field stitching error was measured; we did not attempt to measure the effect of scale stitching errors.

III. RESULTS AND DISCUSSION

A. Baseline performance

Baseline waveguide performance is shown in Fig. 4. Over five months of fabrication, the 66 baseline die measured show a consistent waveguide loss of 4 dB/cm, with a standard deviation of 0.7 dB/cm. While not approaching the lowest reported loss for silicon waveguides, these losses are suitable for device development and design verification. Moreover, for meaningful prototyping, consistent performance is of primary importance.

B. Fundamental writing parameters

Linear waveguides were, of course, unaffected by the polygon digitization used, since linear waveguides are represented by a rectangle specified by only four corner points, and had a mean loss of 4.2 dB/cm. When comparing polygon approximations using 600 and 2400 points-per-circle, the curved waveguides showed an improvement with the higher number of polygon points from 12.7 to 11.5 dB/cm, as shown in Fig. 5. The exposure time was identical for the two
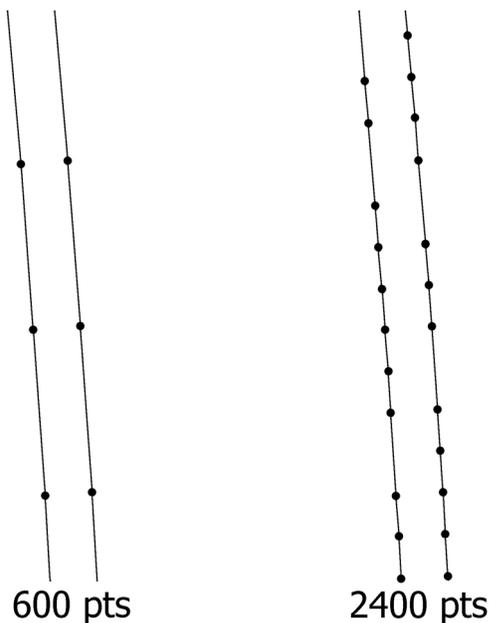

FIG. 3. CAD representations of a curved waveguide segment approximated by polygons using 600 and 2400 points-per-circle, with polygon vertices highlighted.
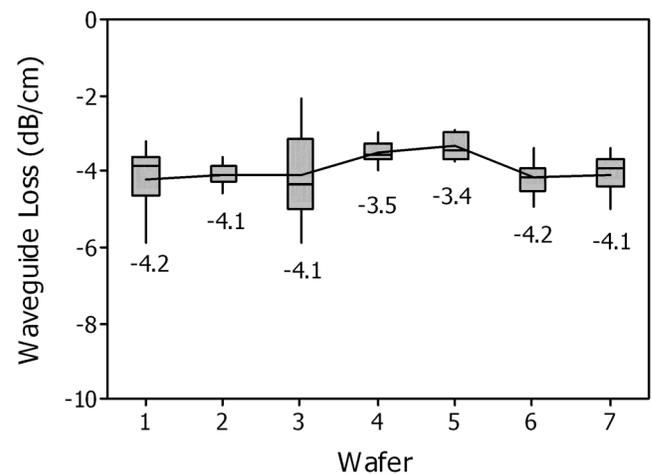

FIG. 4. Box plot showing a baseline process consistency of waveguide loss for 400 nm wide ridge waveguides in SOI. These are quartile box plots; the bottom of the box is at the first quartile, the top of the box is at the third quartile, and the line represents the median of the data.
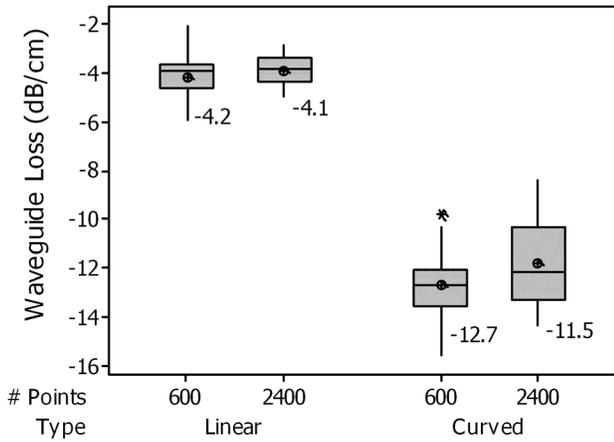
FIG. 5. Box plot of waveguide loss designed using 600 and 2400 points-per-circle polygon approximations.

FIG. 7. Simulations from LayoutBEAMER showing predicted lithographic line edge roughness for different values of the writing grid (shot pitch).

cases, so this higher number of polygon points should be used.

The writing grid, or shot pitch, was varied from 2 to 32 nm, resulting in the waveguide losses shown in Fig. 6. Waveguide performance decreases steadily with increasing grid size, as expected with the increasing line edge roughness expected from a coarser writing grid. Figure 7 shows simulated line edge profiles for the varying shot pitch values, generated by the LayoutBEAMER software.[16] With our equipment set, we cannot reliably characterize the physical line edge roughness to directly confirm these simulations. There is no throughput difference with a varying writing grid, so the clear recommendation is to use the finest writing grid possible for best performance, as one would intuitively assume.

The comparison of the waveguide loss with beam current is shown in Fig. 8. Linear waveguide loss is unaffected at 4.2 dB/cm for either 2 or 8 nA, while curved waveguides showed an improvement in loss from 12.6 to 10.6 dB/cm. Moreover, exposure time per die decreased by nearly a factor of 3, from 14.3 to 4.7 min per die. We speculate that the improved loss is due to smoother sidewall edges, from the increased beam diameter, and process blur from the higher
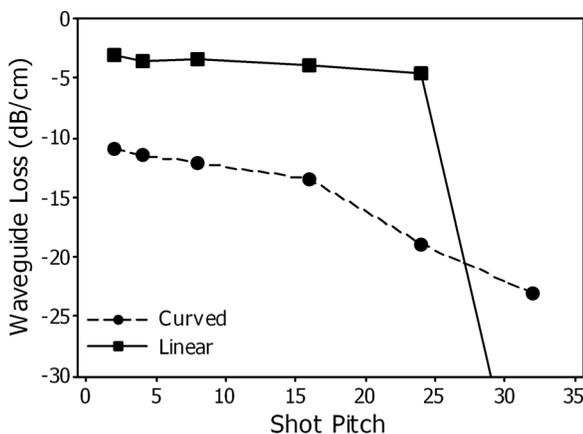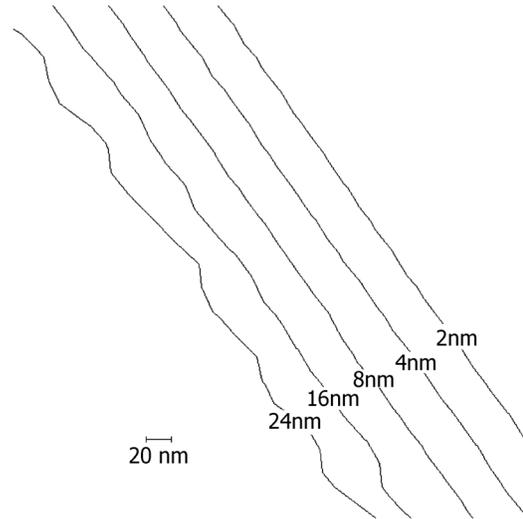
beam current. While the combination of lower loss and faster throughput using larger beam currents seems ideal, the larger beam diameter will reduce the ultimate resolution, resulting in a larger minimum feature size. In this study, the smallest written line is 400 nm and the narrowest gap is 240 nm, so we are not taxing the process resolution, however, other photonic components such as slot waveguides and photonic crystals may demand the higher resolution afforded by the smaller beam current. Additional study will be needed to determine the optimum conditions when smaller features are required.

C. Averaging techniques

The averaging techniques evaluated, field overlap and field shift, both showed improvements to waveguide loss; field shift writing provided 3 dB/cm improvement for curved waveguides, as plotted in Fig. 9. Field shift writing was consistently better than simple overlap writing; this is expected because field shift writing not only averages, over time, the noise from the system and environmental sources, but also

FIG. 6. Measured waveguide loss for varying writing grid or shot pitch, for linear and curved waveguides.
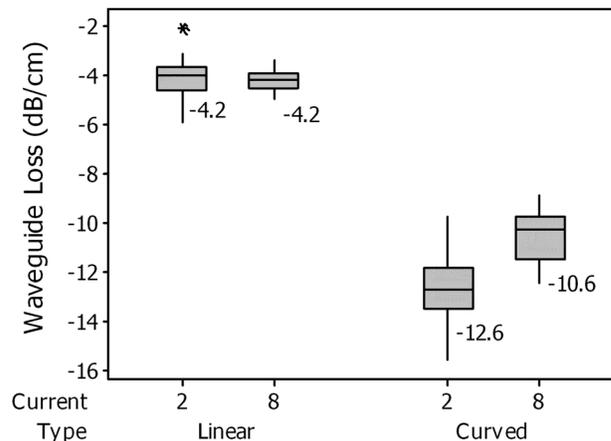

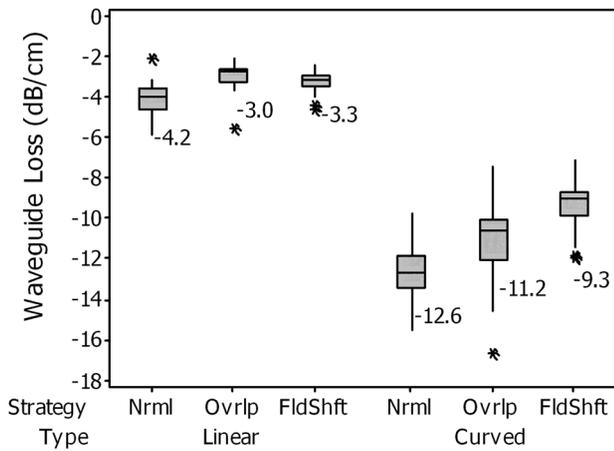FIG. 8. Box plot of waveguide loss for 2 and 8 nA beam currents, for linear and curved waveguides.

FIG. 9. Box plot of waveguide loss for averaging strategies: normal (no averaging), overlap, and field shift, for both linear and curved waveguides.

spatial aberrations in the deflection system, resulting in both smoother edges and reduced field stitch errors.[17] The use of field shift writing increased die writing time by only a few percent, from 14.1 to 14.5 min per die. Although field shift writing requires twice as many stage moves per die, each stage move is only half the distance of those in normal writing, and for our relatively dense test pattern, the die exposure time is dominated by shape writing, not stage moves. Therefore, field shift writing shows a substantial improvement in waveguide loss with a modest increase in writing time. We have since adopted field shift writing as standard practice for our photonics process.

D. Final lens selection

The nanolithography (5th) lens mode, with its smaller deflection field, finer placement grid, and shorter working distance, showed significant improvements in waveguide loss in all cases, both with and without field shifting, as shown in Fig. 10, but with a throughput reduction by about a factor of 2. The large improvements seen with the small-field mode, particularly in the curved waveguides, hint that a primary source of loss-inducing edge roughness is deflection
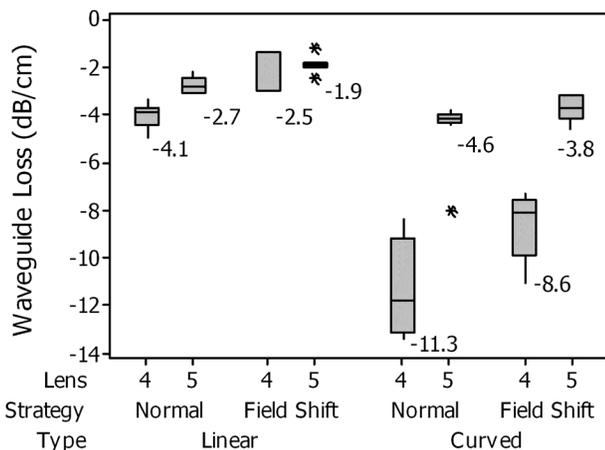

FIG. 10. Box plot of waveguide loss using 4th and 5th lens writing modes, normal and field shift writing, for linear and curved waveguides.
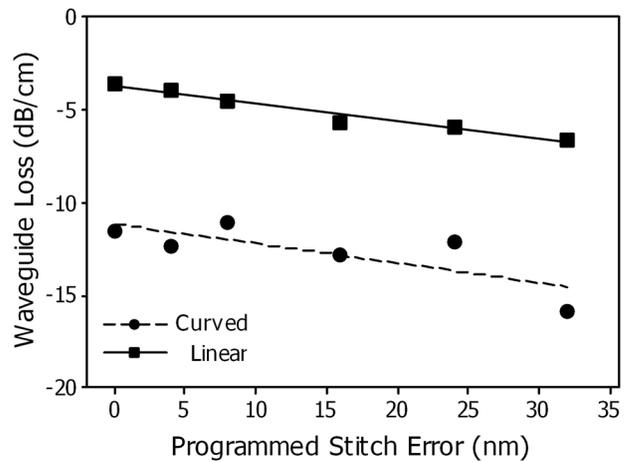
FIG. 11. Dependence of waveguide loss on the magnitude of programmed stitching errors. For both linear and curved waveguides, the slope indicates shear stitching errors; add about 0.1 dB of loss for each nanometer of stitching error.

noise in the shape placement deflection system. The primary difference between the lens modes is a reduction in the deflection range by a factor of 8; shape placement noise should also reduce by this factor, while other sources of loss-inducing roughness remain constant. In all cases, the 4th- and 5th-lens die were written intermixed on the same substrate, so differences in waveguide loss are purely due to the exposure step, not elsewhere in the process. When utilized together, the combination of 5th lens mode and field shift averaging produced the lowest-loss waveguides in this study.

E. Simulated stitching errors

The simulation of field stitch errors by programmed offsets in the pattern provides an estimate of ~0.1 dB/cm additional loss for each nm of field stitch error, for both linear and curved waveguides, as shown in Fig. 11. Although our university lab does not have the capability to reliably measure stitching errors as small as expected of our e-beam system, Leica LMS IPRO measurements of wafers during tool acceptance showed mean stitch errors of 5 nm with a standard deviation of 5.2 nm. Given this loss sensitivity to field stitch errors previously determined, this would indicate that field stitch errors are likely a relatively small source of loss in our waveguides, <1 dB/cm, and that other loss mechanisms such as sidewall roughness are still dominant.

IV. SUMMARY AND CONCLUSIONS

We have explored a variety of EBL writing conditions and their impact on waveguide loss for silicon waveguides, along with their impact on writing throughput. Collectively, these results guide us to optimizing writing conditions for reasonably low loss and high throughput, and give us quantitative estimates of the tradeoffs of the variables. Writing conditions that result in smoother waveguide sidewalls, such as smaller writing grid, higher beam current, or averaging all show improvement in waveguide loss. In our case, the

smaller writing field size gives the largest gain in waveguide performance, especially for curved waveguides, most likely due to reduced shape placement noise. This optimized process is now in use for prototyping of silicon photonic components, supporting basic photonic device research, along with providing design feedback for larger-scale system designs for integrated silicon photonics endeavors. Ongoing process development work includes extending the process to higher-resolution features such as photonic crystals and sub-60 nm wide slots, and multiple layer structures including partially etched silicon layers and metal contact layers.

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